

JOYNED

AUDIO.
NETWORK.
TECHNOLOGY.

MT32-EVK - MILAN To TDM - Datasheet

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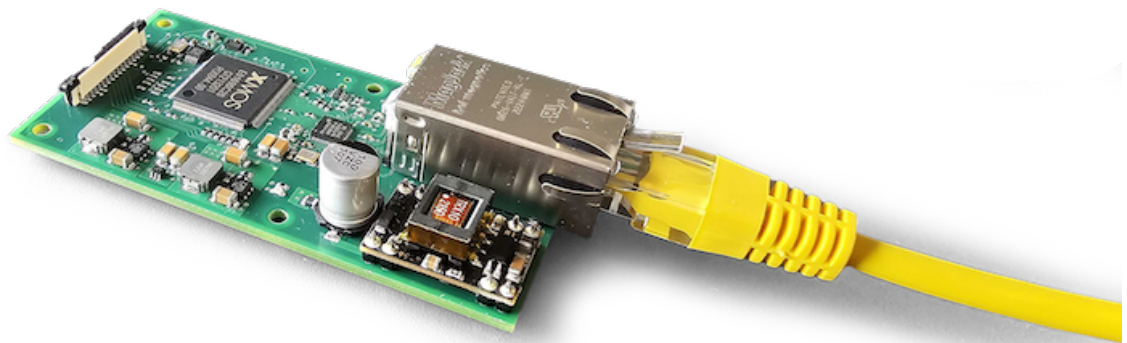
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Brief

This Milan module is your go-to tool for starting audio network developments. Its compact size makes it both convenient and cost-effective for building your Milan product. Optional output cards provide the flexibility to adapt to various use cases. Powered by JOYNED's Milan Endpoint Software, it ensures seamless integration, Avnu certification support, and robust performance for live sound, studio production, and commercial AV installations.



Overview

Dimensions

80 mm x 40 mm

Features

- AVB/Milan in/out (1Gbit/100Mbit depending on processor resource usage)
- PoE powered
- TDM audio interface
- JTAG Programming interface
- Power supply for optional IO cards
- Optional GPIOs
- Optional UART control

Product Details

JOYNED Milan Software on MT32

- Full Milan compliance for professional audio over Ethernet.
- Supports up to **16x16 audio channels** and **2x2 streams**.
- Compatible with **sampling rates of 44.1 kHz, 48 kHz, up to 88.2 kHz, and 96 kHz**.
- Simplified integration process with XMOS microcontrollers, ensuring a reliable and solid foundation.
- Functional verification support provided by JOYNED for meeting all professional standards.

Microcontroller

XMOS xCORE-200 XE216: A high-performance, 16-core microcontroller designed for time-sensitive applications:

- Dual 32-bit RISC cores running at up to 500 MHz.
- Deterministic execution for precise timing.
- Integrated support for networking, I/O, and control applications.
[Learn more about the xCORE-200 XE216¹.](#)

Clock Recovery (PLL)

Cirrus Logic CS2100 or CS2501 for low-jitter clock recovery, ensuring high-precision synchronization.
[Learn more about the CS2501 PLL².](#)

1. <https://www.xmos.com/xcore-200>

2. <https://www.cirrus.com/products/cs2501/>

Ethernet PHY

AR8035 for reliable transmission and reception of ethernet data.

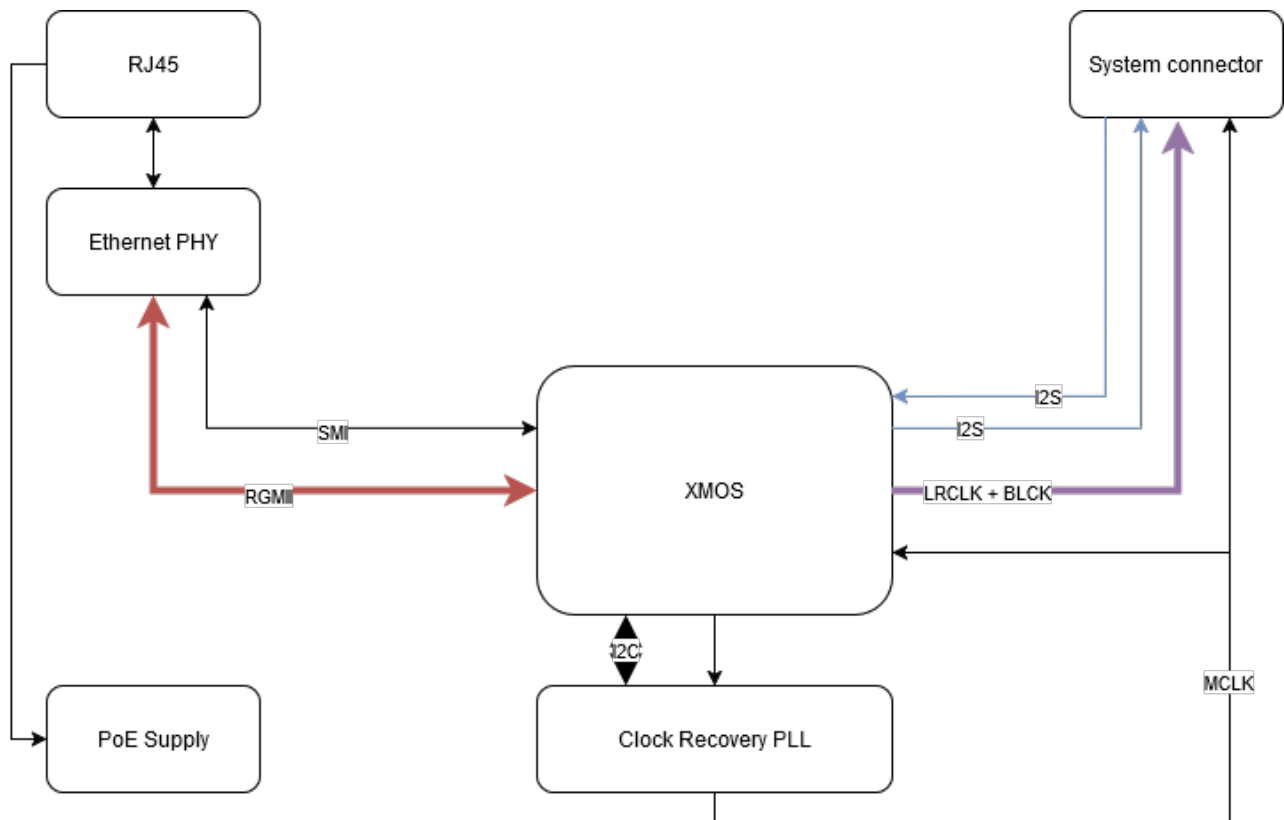
System Connector

- Master Clock
- Serial Audio Interface (LRCLK/FSYNC, BCLK, Data)
- I2C
- GPIOs
- Power 5V and 3.3V

Power Over Ethernet (PoE)

A Silvertel PoE Module powers the whole circuit with enough headroom for peripherals connected through the System connector.

Block Diagram



Pinout

Debug

Connector-Type: TAG-Connect TC2050NL

Pin	Signal name	Signal type
1	XL_DN1	X-Channel
2	XL_DN0	X-Channel
3	XL_UP0	X-Channel
4	XL_UP1	X-Channel
5	GND	GND
6	XSYS_RST_N	Reset
7	TMS	JTag
8	TCK	JTag
9	TDO	JTag
10	TDI	JTag

USB

Connector type: FFC 0.5mm 6 pin

Pin	Signal name	Signal type
1	GND	Ground
2	USB_VBUS	USB

3	USB_ID	USB
4	USB_DP_P	USB
5	USB_DM_N	USB
6	GND	Ground

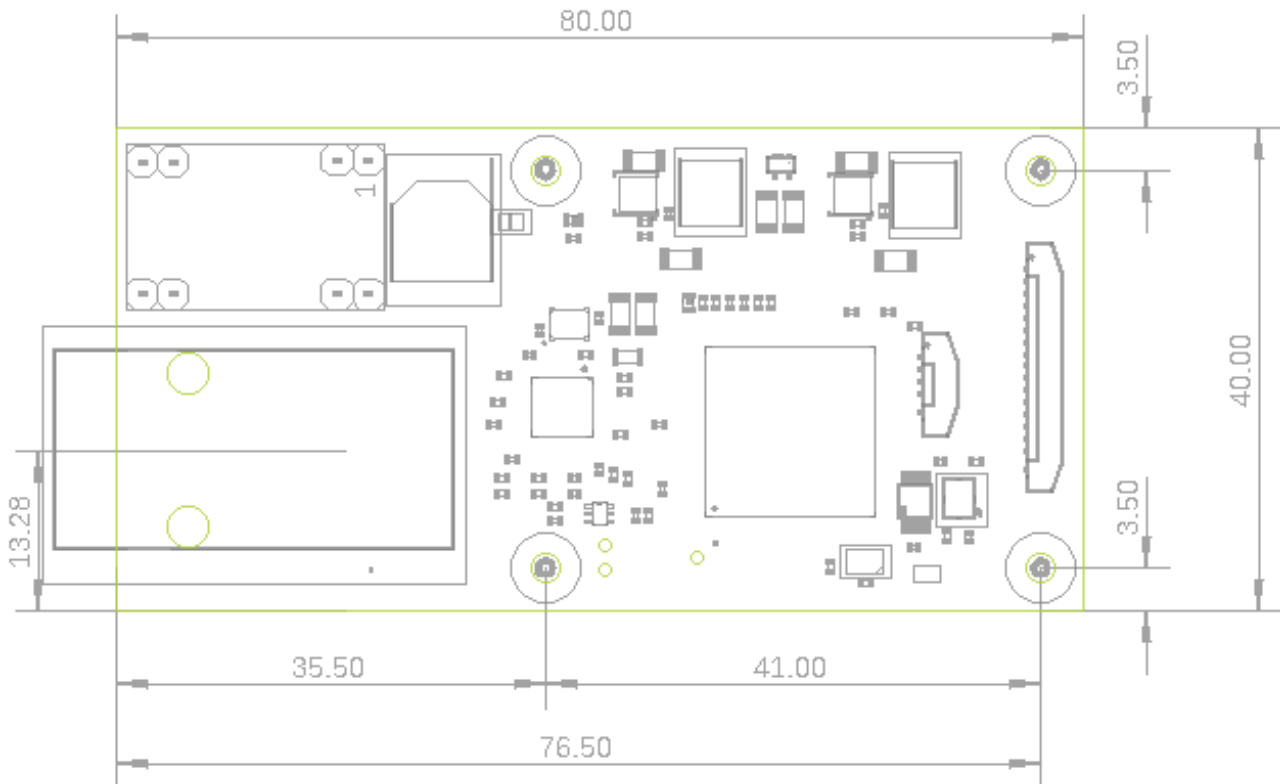
System

Connector type: FFC 0.5mm 30 pin

Pin	Signal name	Signal type
1	5V0	Power-in/out
2	5V0	Power-in/out
3	3V3	Power-out
4	3V3	Power-out
5	GPIO_OUT	GPIO
6	ADC_RST_N_OUT	Reset (out)
7	N.C.	Not connected
8	GND	Ground
9	SDIOD_IN	I2S, Data in/out (default i2s in)
10	GND	Ground
11	SDIOC_IN	I2S, Data in/out (default optical in)
12	GND	Ground

13	SDIOB_OUT	I2S, Data in/out (default i2s out)
14	GND	Ground
15	SDIOA_OUT	I2S, Data in/out (default optical out)
16	GND	Ground
17	SCLK_OUT	I2S, Bit clock out
18	GND	Ground
19	LRCK_OUT	I2S, LR clock out
20	GND	Ground
21	MCLK_OUT	Master clock out
22	GND	Ground
23	SDA	I2C, data
24	SCL	I2C, clock
25	GND	Ground
26	GND	Ground
27	SDIOE_OUT	I2S, Data in/out (default SPDIF-TX)
28	GND	Ground
29	SDIOF_IN	I2S, Data in/out
30	GND	Ground

Mechanical Drawing



Power supply

The AVB base module provides a 5V and a 3,3V supply for extension cards.

Clocking

LRCK_OUT, MCLK_OUT and SCLK_OUT are synchronous clocks to drive I2S or TDM transmission. The AVB base module is always considered to be the master on the bus. Slaving to external clocks is not supported.

I2C

The I2C interface is shared with the CS2300 on the AVB base module. Therefore address 0x4E is reserved and can not be used on the extension cards.

GPIO

Reserved for future use.

Reset

The reset line allows to reset peripherals on the extension cards. The reference firmware pulls the reset line low on initialisation or whenever a sample rate change occurs.

Serial Data Lines

The module provides 6 serial data lines on the 30 pin FFC system connector named SDIOx_yy. X ranging from A to F and yy giving the default signal direction. This lines can be synchronously clocked with LRCK_OUT, MCLK_OUT and SCLK_OUT when used as I2S or TDM lines. Alternatively they can be freely programmed to serve as GPIO or any other protocol like I2C, SPI, etc.

The signal direction can be freely configured, but needs software and hardware modifications.

Ethernet

MAC Address

Note: In hardware Version 1 and 2 MAC addresses are taken from the set of Locally Administered Address Ranges! Hardware version 3 provides unique MAC addresses. The XMOS toolchain with the programmer can be used to burn vendor specific MAC addresses.

Provided firmware options

With the I2S/TDM reference firmware I2S/TDM data is provided on SDIOD_IN (**default i2s in**) and SDIOB_OUT (**default i2s out**).

With the ADAT reference firmware SDIOC_IN is used for the optical input and SDIOA_OUT is used for the optical output.

With the AES3-EBU reference firmware SDIOA_OUT is used for the AES3/SPDIF output.

With the PMOD-AMP reference firmware I2S data is provided on TBD.