JOYNED
AUDIO.
NETWORK.
TECHNOLOGY.

XM2-EVK "Panda Board" - Evaluation Kit for MILAN Software on XMOS - Datasheet

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(AVB Extension for XMOS XK-EVK-XE216)

Hardware Rev. V1

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Brief

The JOYNED XM2-EVK is an evaluation platform designed for developers who aim to prototype software for their own AVB/Milan products. Powered by JOYNED's Milan Endpoint Software, it ensures seamless integration, Avnu certification support, and robust performance for live sound, studio production, and commercial AV installations.


JOYNED

Overview

The JOYNED XM2-EVK provides manufacturers and developers with a robust platform to design, test, and prototype AVB/Milan-compatible products.

Powered by JOYNED XM2 - MILAN Software

JOYNED Milan Software, designed for XMOS microcontrollers, integrates smoothly with the Milan standard for audio over Ethernet. It supports up to 64x64 audio channels, stream counts of 8x8, and sampling rates of up to 96 kHz. Whether for **live sound**, **studio production**, or **commercial installations**, the JOYNED Software simplifies development, bringing network technology to more places.

JOYNED Milan software can be licensed directly. Learn more at JOYNED's website[1].

Dimensions

200 mm x 120 mm

Features

- **Fully Milan-Compliant**: Supports professional AVB/Milan networking for seamless audio-over-Ethernet integration.
- **High Channel Count**: Handles up to 64x64 audio channels with 8x8 stream support.
- **Flexible Sampling Rates**: Supports 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz for versatile audio applications.
- **Deterministic Processing**: XMOS xCORE-200 XE216 microcontroller ensures precise timing and low-latency performance.
- **Low-Jitter Clock Recovery**: Cirrus Logic CS2100/CS2501 PLL provides accurate synchronization for high-quality audio.
- **High-Fidelity Audio Codec**: Cirrus Logic CS4272 with 24-bit ADC/DAC and up to 120 dB dynamic range.
- **Comprehensive Connectivity**: Includes Master Clock, Serial Audio Interface, I2C, GPIOs, and Power (5V/3.3V).
- **Reliable Ethernet**: Microchip KSZ9131 Ethernet PHY for stable data transmission.
- **Development-Friendly**: Ideal for manufacturers and developers prototyping AVB/Milan-compatible products.

Product Details

JOYNED XM2 - MILAN Software

- Full Milan compliance for professional audio over Ethernet.
- Supports up to **64x64 audio channels** and **8x8 streams**.
- Compatible with **sampling rates of 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz**.

1. https://www.joyned.at/milan-software-for-xmos

- Simplified integration process with XMOS microcontrollers, ensuring a reliable and solid foundation.
- Functional verification support provided by JOYNED for meeting all professional standards.

Microcontroller

- **XMOS xCORE-200 XE216**: A high-performance, 16-core microcontroller designed for time-sensitive applications:
  - Dual 32-bit RISC cores running at up to 500 MHz.
  - Deterministic execution for precise timing.
  - Integrated support for networking, I/O, and control applications.
    Learn more about the xCORE-200 XE216[2].

Clock Recovery (PLL)

Cirrus Logic CS2100 or CS2501 for low-jitter clock recovery, ensuring high-precision synchronization.
Learn more about the CS2501 PLL[3].

Codec

Cirrus Logic CS4272: A high-performance, 24-bit audio codec with:

- **24-bit analog-to-digital (ADC) and digital-to-analog conversion (DAC)**.
- Dynamic range up to **114 dB** for ADC and **120 dB** for DAC.
- Support for sampling rates of **up to 192 kHz**, ensuring pristine audio fidelity.
- Integrated features such as volume control and mute for enhanced audio control.
  Learn more about the CS4272[4].

System Connector

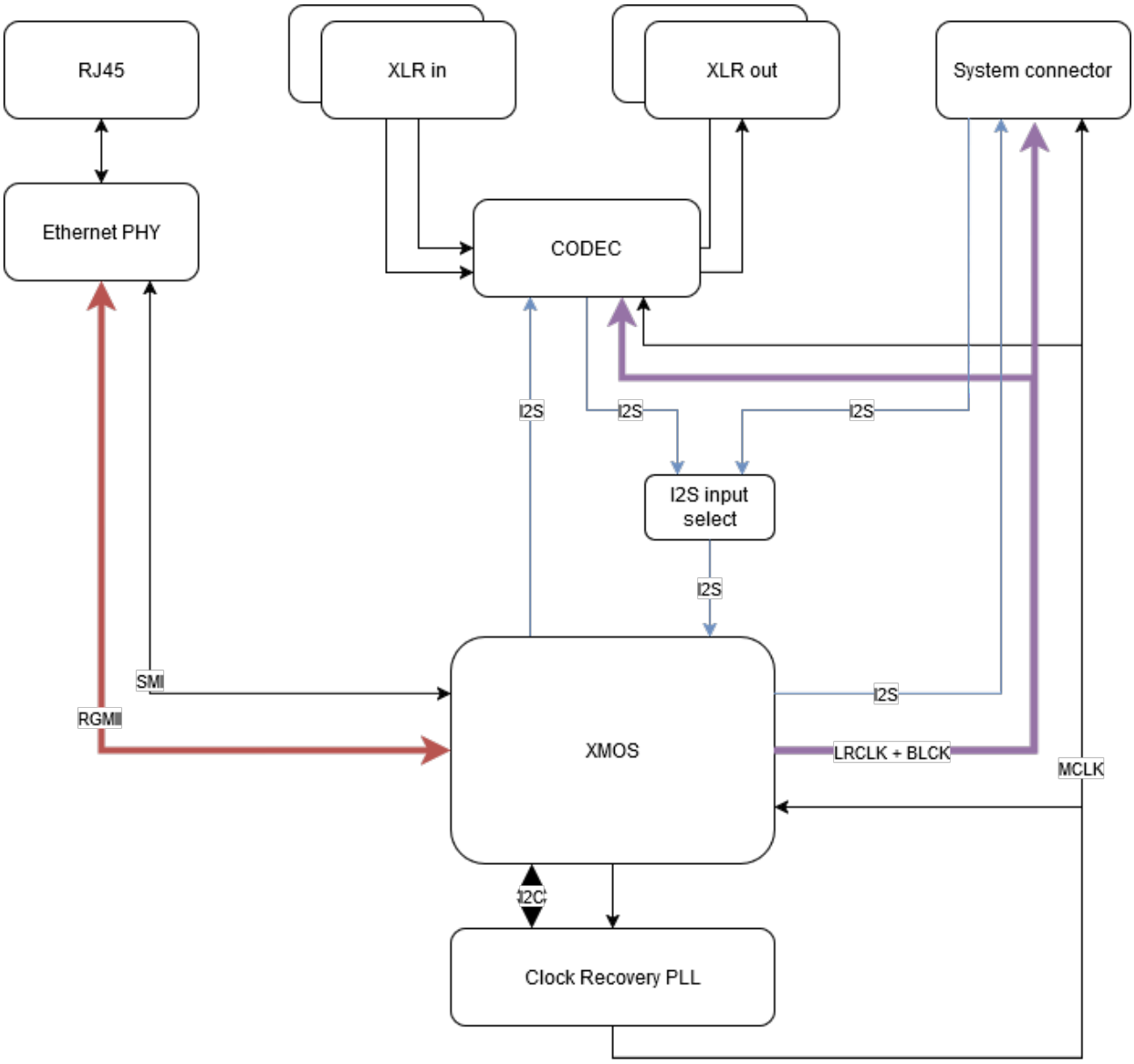
- Master Clock
- Serial Audio Interface (LRCLK/FSYNC, BCLK, Data)
- I2C
- GPIOs
- Power 5V and 3.3V

Ethernet PHY

Microchip KSZ9131 for reliable transmission and reception of Ethernet Data. (Older revision may still include the AR8035 instead of the KSZ9131).

2. https://www.xmos.com/xcore-200
3. https://www.cirrus.com/products/cs2501/
4. https://www.cirrus.com/products/cs4272/

Block diagram



Pinout

System

To interface with existing JOYNED modules, the extension card shall provide a System connector with the following pinout.

Connector type: FFC 0.5mm 30 pin

Pin	Signal name	Signal type
1	5V0	Power-in/out
2	5V0	Power-in/out
3	3V3	Power-out
4	3V3	Power-out
5	GPIO_OUT	GPIO
6	ADC_RST_N_OUT	Reset (out)
7	N.C.	Not connected
8	GND	Ground
9	SDIOD_IN	I2S, Data in/out (**default i2s in**)
10	GND	Ground
11	SDIOC_IN	I2S, Data in/out (**default optical in**)
12	GND	Ground
13	SDIOB_OUT	I2S, Data in/out (**default i2s out**)
14	GND	Ground
15	SDIOA_OUT	I2S, Data in/out (**default optical out**)

16	GND	Ground
17	SCLK_OUT	I2S, Bit clock out
18	GND	Ground
19	LRCK_OUT	I2S, LR clock out
20	GND	Ground
21	MCLK_OUT	Master clock out
22	GND	Ground
23	SDA	I2C, data
24	SCL	I2C, clock
25	GND	Ground
26	GND	Ground
27	SDIOE_OUT	I2S, Data in/out (default SPDIF-TX)
28	GND	Ground
29	SDIOF_IN	I2S, Data in/out
30	GND	Ground

Connection to xCore-200 eXplorer J3

Note: See xCORE-200 explorerKIT Hardware Manual - Chapter 3

No connections assigned!

Pin	Signal name	XMOS pin name	Signal type

1	GND		Ground
2		X1D35	
3	GND		Ground
4		X1D38	
5	GND		Ground
6		X1D39	
7	GND		Ground
8		X1D16	
9	GND		Ground
10		X1D17	
11	GND		Ground
12		X1D18	
13	GND		Ground
14		X1D19	
15	GND		Ground
16		X1D14	
17	GND		Ground
18		X1D15	
19	GND		Ground
20		X1D20	

21	GND		Ground
22		X1D21	
23	GND		Ground
24		X1D04	
25	GND		Ground
26		X1D05	
27	GND		Ground
28		X1D06	
29	GND		Ground
30		X1D07	
31	GND		Ground
32		X1D02	
33	GND		Ground
34		X1D03	
35	GND		Ground
36		X1D08	
37	GND		Ground
38		X1D09	
39	GND		Ground
40		X1D00	

41	GND		Ground
42		X1D01	
43	GND		Ground
44	GND		Ground

Connection to xCore-200 eXplorer J1

Note: See xCORE-200 explorerKIT Hardware Manual - Chapter 3

Pin	Signal name	XMOS pin name	Signal type
1		X0D31	
2	GND		
3	GPIO	X0D30	GPIO
4	GND		
5		X0D29	
6	GND		
7		X0D28	
8	GND		
9		X0D33	
10	GND		
11	ADC_RST_N	X0D32	ADC / DAC Reset line
12	GND		

13		X0D27	
14	GND		
15		X0D26	
16	GND		
17	SDIOD	X0D35	I2S Data line
18	GND		
19	SDIOC	X0D34	I2S Data line
20	GND		
21	SDIOB	X0D25	I2S Data line
22	GND		
23	SDIOA	X0D24	I2S Data line
24	GND		
25		X0D19	
26	GND		
27		X0D18	
28	GND		
29		X0D17	
30	GND		
31		X0D16	
32	GND		

33	SCLK	X0D23	I2S / TDM Bitclock
34	GND		
35	LRCLK	X0D22	I2S Wordclock / TDM Framesync
36	GND		
37	MCLK_XCORE0	X0D13	Master clock to XMOS
38	GND		
39	TP1	X0D12	Test
40	GND		
41		X0D21	
42	GND		
43		X0D20	
44	GND		
45		X0D15	
46	GND		
47		X0D14	
48	GND		
49		X0D09	
50	GND		
51		X0D08	
52	GND		

53	SDA	X0D03	I2C
54	GND		
55	SCL	X0D02	I2C
56	GND		
57	PLL_SYNC_SiLabs_C	X0D39	Clock reference to Silabs.
58	GND		
59	PLL_SYNC_Renesas	X0D38	Clock reference to Renesas.
60	GND		
61	PLL_SYNC_SiLabs_B	X0D37	Clock reference to Silabs.
62	GND		
63	PLL_SYNC_CS2100	X0D36	Clock reference to CS2100.
64	GND		

Analog out L

Connector type: XLR male

E.g. Neutrik NC3MAAH

Pin	Signal name	Signal type
1		
2		
3		

Analog out R

Connector type: XLR male

E.g. Neutrik NC3MAAH

Pin	Signal name	Signal type
1		
2		
3		

Analog in L

Connector type: XLR female

E.g. Neutrik NC3FAAH

Pin	Signal name	Signal type
1		
2		
3		

Analog in R

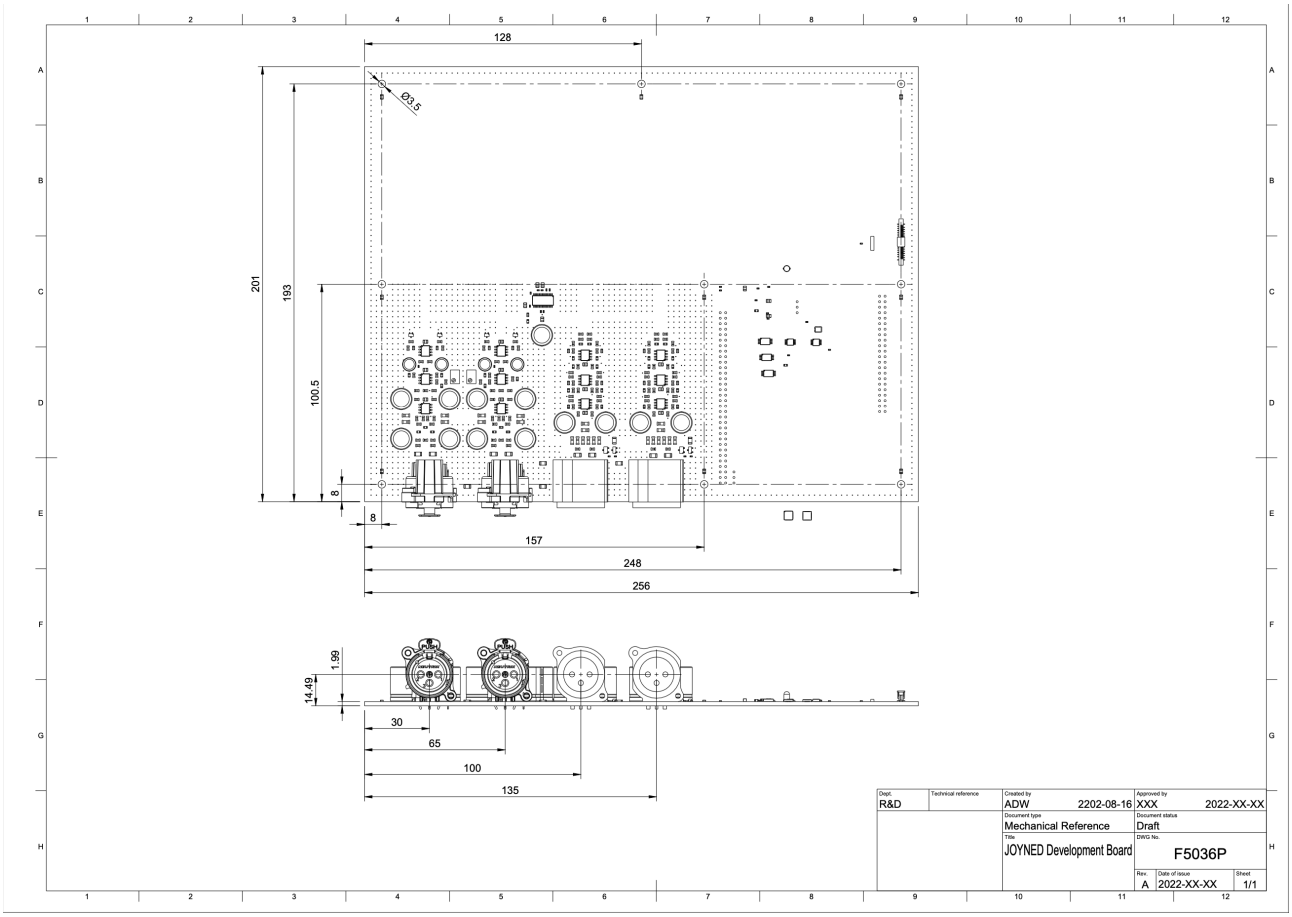
Connector type: XLR female

E.g. Neutrik NC3FAAH

Pin	Signal name	Signal type
1		
2		
3		

Mechanical drawing

Width: To fit into a 9,5” enclosure. (Including xCore-200 explorer board)



Power supply

⚠ A DC-Input of 5.8V to 5.9V is required in Version 1. Absolute maximum rating is 6V.

A wider input voltage range is provided from Version 2 onwards.

Recommended Wall mount AC Adapter

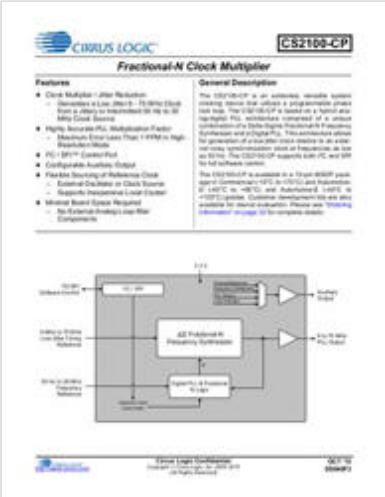
(from Version 2 onwards)

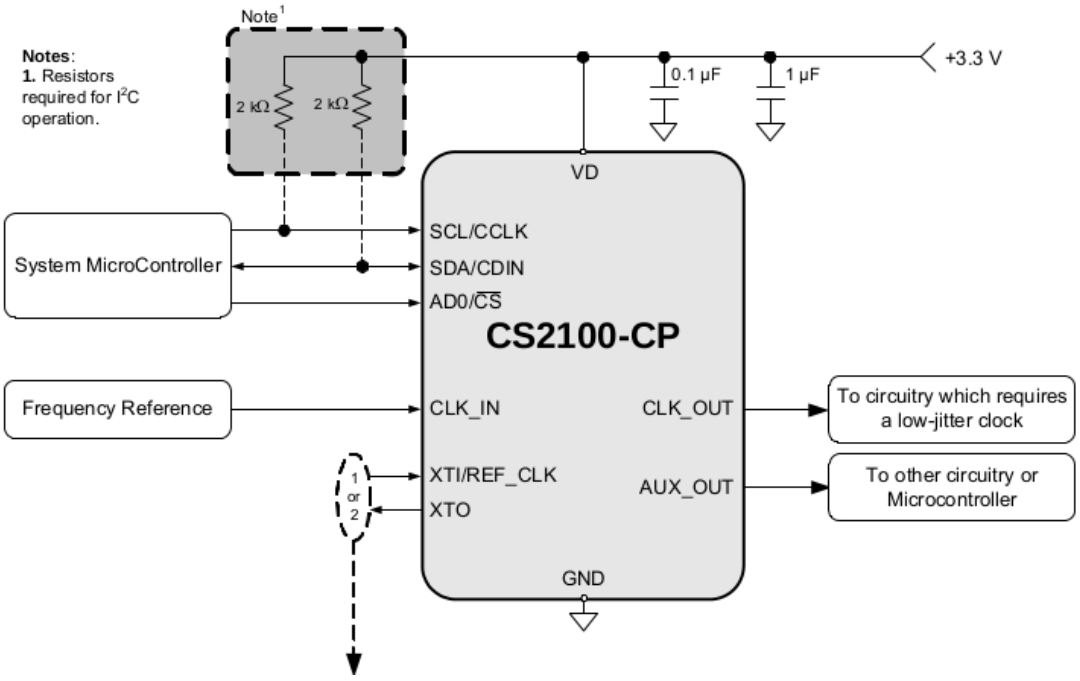
https://www.mouser.at/ProductDetail/Phihong/PSC15R-090-R?qs=GBLSl2Akirsh1YBr54Nkdw%3D%3D + https://www.mouser.at/ProductDetail/Phihong/RPE-AB01B-H?qs=zW32dvEIR3sKOd9e1WTTzg%3D%3D or https://www.mouser.at/ProductDetail/Phihong/RPS-AB01B-H?qs=zW32dvEIR3uk2nw48BVOuw%3D%3D

Clocking

LRCK_OUT, MCLK_OUT and SCLK_OUT are synchronous clocks to drive I2S or TDM transmission. The AVB base module is always considered to be the master on the bus. Slaving to external clocks is not supported.

CS2100CP

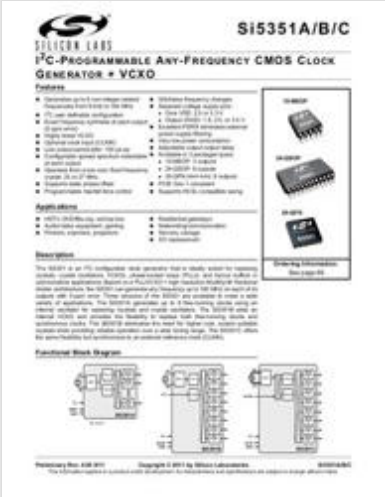




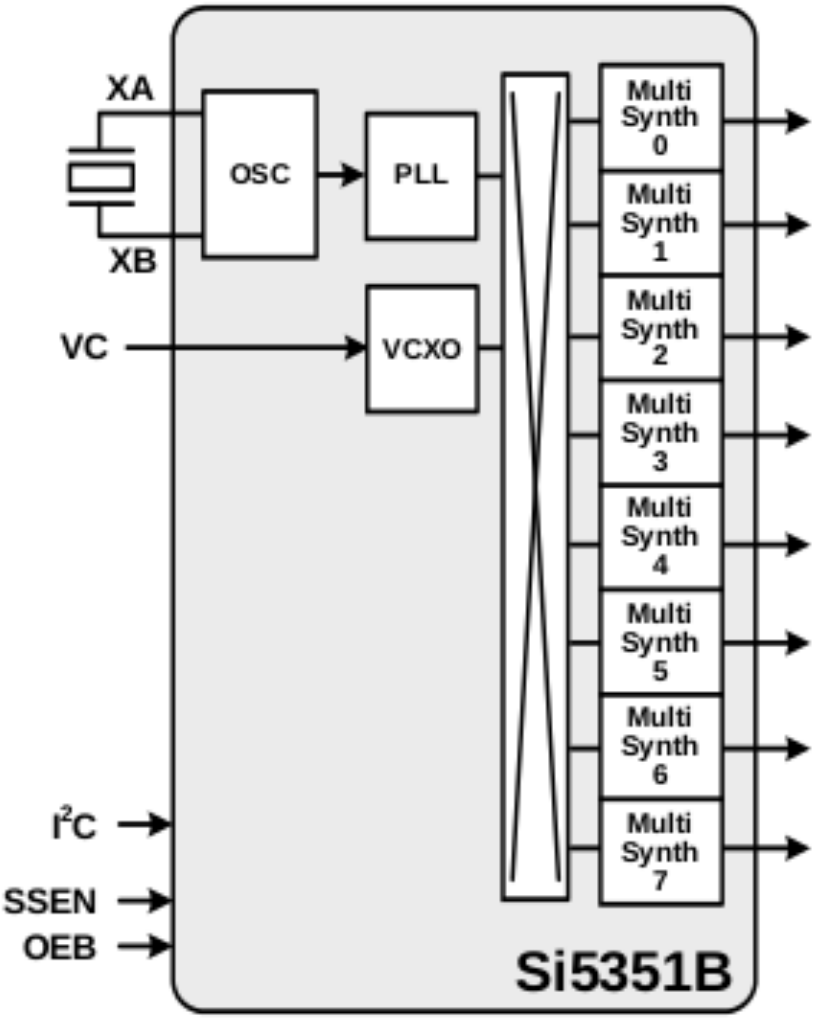
- Similar to XMOS reference design.
- No Multiplexer for clock selection needed.
- CLK_IN is connected to PLL_SYNC_CS2100
- CLK_OUT is used to feed MCLK_* signals

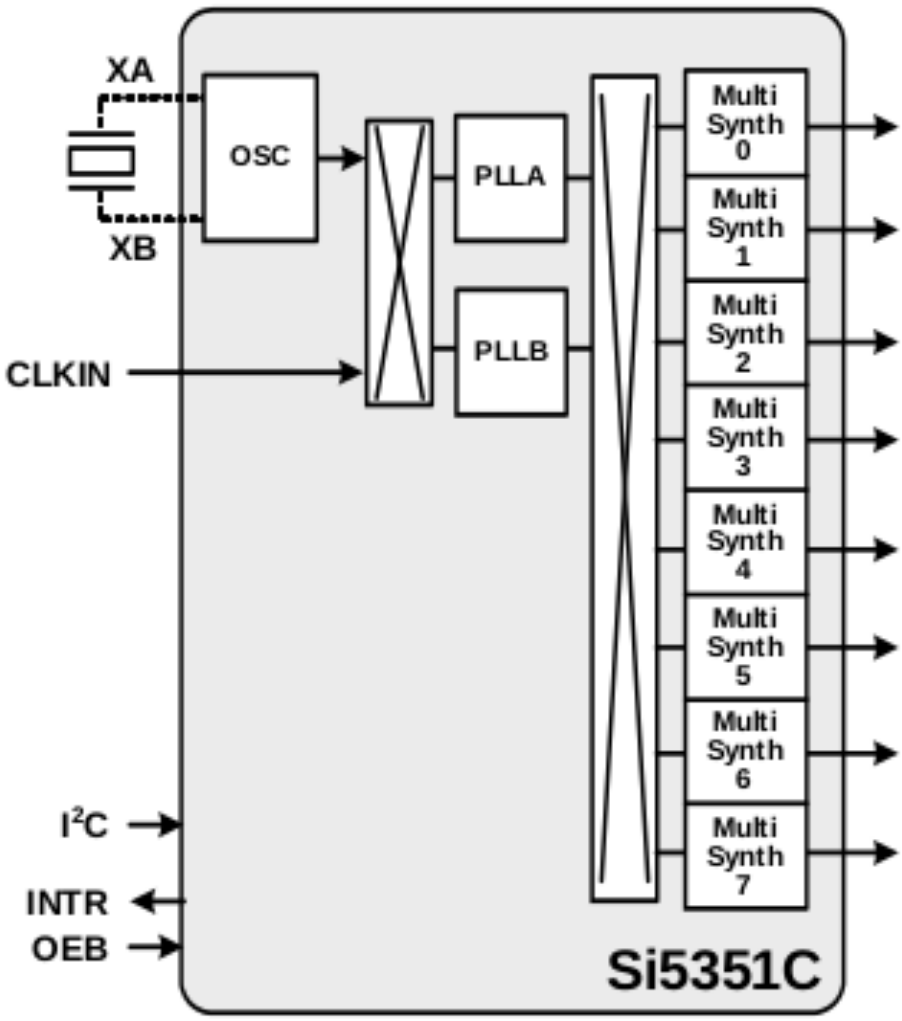
- Control per I2C

SiLabs Si5351B/C


Si5351A/B/C

I²C-PROGRAMMABLE ANY-FREQUENCY CMOS CLOCK GENERATOR + VCXO


XA
XB
VC
OSC
PLL
VCXO
Multi Synth 0
Multi Synth 1
Multi Synth 2
Multi Synth 3
Multi Synth 4
Multi Synth 5
Multi Synth 6
Multi Synth 7
I²C
SSEN
OEB
Si5351B



- Use the Voltage control (VC) input. A PWM will be generated from the XMOS on PLL_SYNC_SiLabs_B.
- Alternatively use clock input (CLKIN) from XMOS on PLL_SYNC_SiLabs_C.
- controlled per I2C.
- Outputs shall be accesible on testpoints (at least 1 to 4)

Only difference between the B and the C variant is the usage of pin 3 and pin 6. Please connect PLL_SYNC_SILABS_C to pin 6 (SSEN / CLKIN). Then we have the freedom to experiment with both variant of the SI5351.
usage of pin3: Variant B = VC, Variant C = INTR
usage of pin6: Variant B = SSEN, Variant C = CLKIN

I2C

The I2C interface is shared with the CS2100 on the AVB extension card. Therefore address 0x4E is reserved and must not be used by other components or on other extension cards.

- [ ] I2C address of the ADC/DAC TBD
- [ ] I2C address of the SiLabs TBD

GPIO

Reserved for future use.

Reset

The reset line allows to reset peripherals on the extension cards. The reference firmware pulls the reset line low on initialisation or whenever a sample rate change occurs.

Serial Data Lines

The module provides 6 serial data lines on the 30 pin FFC system connector named SDIOx_yy. X ranging from A to F and yy giving the default signal direction. This lines can be synchronously clocked with LRCK_OUT, MCLK_OUT and SCLK_OUT when used as I2S or TDM lines. Alternatively they can be freely programmed to serve as GPIO or any other protocol like I2C, SPI, etc.

The signal direction can be freely configured, but needs software and hardware modifications.

Attachments